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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,643	11/29/2001	Keiji Inoue	36856.585	8176

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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,643	INOUE ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 10-14* is/are allowed.

6)☒ Claim(s) *5-9 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *20 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1, 5, 10, and 15 are objected to because of the following informalities:

Claim 1, line 15, the limitation of "mother substrate" is unclear. Examiner suggests to change to –motherboard--.

Claim 5, line 3, the limitation of "each having connecting" is unclear. Examiner suggests to change to –each having connecting members--.

Claim 5, line 8, the limitation of "said connecting pad" should be change to –said connecting pads--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, lines 10-13, it is unclear. The phrase of "said plurality of module substrates...are sequentially offset from one another...in a stacking direction" is not understood. What does applicant mean of "the direction of arrangement of said connecting terminals" and "a stacking direction" Examiner assumes that "the plurality of

module substrates are stacked and sequentially offset from one another on the motherboard, so that the connecting terminals of the module substrate are aligned and electrically connected to the connecting pads of the motherboard" and by applying art as below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 5-6, 8, 15, and 17, insofar as in compliance with 35 U. S. C. 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Fogal et al. (U. S. Patent 6,313,998).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and not to be taken as limiting.

As best understood to claim 5, Fogal et al. disclose a module substrate mounting structure (10, column 3, lines 36-38) as shown in figures 1-4 comprising:

a motherboard (substrate 12, column 3, line 38) inherently having connecting pads (not shown) disposed on a surface thereof; and

a plurality of module substrates (18, 28, figure 1, or 18, 28, and 54, figure 4) each having connecting members (44, 50, 56-figure 4) attached to a surface thereof via connecting terminals (26, 36,and 60, column 3, lines 57, 62,column 5, line 5) disposed on each of said plurality of module substrates (18, 28, and 54); wherein

said module substrates (18, 28, 54) are stacked with a space therebetween on said motherboard (see figures 1 and 4), said connecting members (44, 50, and 56) of said module substrates (18, 28, and 54) are electrically connected to the to said connecting pads on said motherboard (12), said connecting terminals are arranged along an edge portion of each of said module substrates,

said module substrates are stacked on said motherboard and are sequentially offset from one another with said connecting terminals aligned with each other in an arrangement of said connecting terminals so that said edge portions with said connecting terminals disposed thereon are aligned with one another, and said connecting pads (pads on the substrate 12) electrically connected to said connecting terminals (26, 36,and 60) of said substrates via said connecting members (wires 44, 50, 56) are arranged in the same row.

Regarding claim 6, Fogal et al. disclose the structure as shown in figures 1-4 wherein a lower substrate (18-figure 4) recognition mark is located on an exposed portion of a lower module substrates of said plurality of module substrates

Regarding claims 8, 17, Fogal et al disclose the structure (10) wherein a ratio of a length to a width of each of said module substrates is within a range of about 1/3 to about 1/1, see figures 2-3.

As to claim 15, Fogal et al. disclose a module substrate mounting structure (10, column 3, lines 36-38) as shown in figures 1-4 comprising:

a motherboard (substrate 12, column 3, line 38) inherently having connecting pads (not shown) disposed on a surface thereof; and

a plurality of module substrates (18, 28, figure 1, or 18, 28, and 54, figure 4) each having connecting members (44, 50, 56-figure 4) attached to a surface thereof via connecting terminals (26, 36,and 60, column 3, lines 57, 62,column 5, line 5) disposed on each of said plurality of module substrates (18, 28, and 54); wherein

said module substrates (18, 28, 54) are stacked with a space therebetween on said motherboard (see figures 1 and 4), said connecting members (44, 50, and 56) of said plurality of module substrates (18, 28, and 54) are electrically connected to the to said connecting pads on said motherboard (12, see figures 1 and 4), said connecting terminals are arranged along a pair of edge portions (see figures 2 and 3) of each of said module substrates so that the direction of arrangement of said connecting terminal of an upper substrate is substantially perpendicular to the direction of arrangement of said connecting terminals of a lower substrate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. ('886) in view of Mandai et al. (U. S. Patent 5,726,612).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and not to be taken as limiting.

Fogal et al. disclose all of the limitations of the claimed invention as detailed above, except for the module substrates have a nozzle suction area that is arranged to be drawn by a component transporting suction nozzle.

Mandai teach a nozzle suction (3) formed electronic components on a substrate (1) disclosed in figure 1.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a nozzle suction in the structure of Fogal et al. as taught by Mandai in order to place components mounting on a PCB and also prevent ESD for the components when they are mounted on PCB.

8. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. ('886) in view of Prior Art (figure 12, admitted by applicant, hereafter PA).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and not to be taken as limiting.

Fogal et al. disclose all the limitations of the claimed invention as detailed above, except for each of said module substrates having a converter power supply circuit.

PA (figure 12) shows a module substrate (49), which is a DC-DC converter device.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a module substrate having a converter power supply circuit in the structure of Fogal et al. as taught by Mandai in order to convert input DC voltage and current into output DC voltage and current of the module substrate mounting structure.

Allowable Subject Matter

9. Claims 1-4, and 10-14 are allowed.

The following is an examiner's statement of reasons for allowance:

The references cited in this and the previous office action disclose a module substrate mounting structure having a motherboard and a plurality of module substrate, and some other claim elements. However, they do not disclose a plurality of rows of connecting pads of the motherboard are arranged to be sequentially offset from one another from an inner region of the motherboard where the module substrates are mounted toward an outer region of the motherboard, connecting members of an upper module substrate of the plurality of module substrates are electrically connected to an

outer row of connecting pads and connecting members of a lower module substrate of the plurality of module substrates are electrically connected to an inner row of connecting pads disposed inwardly of the outer row of connecting pads.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Glenn et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
September 02, 2003.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2300